

**Amendments to the Claims:**

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

**Listing of Claims:**

- 5 1. (currently amended) A chip circuit component comprising:  
a semiconductor substrate;  
a metallization structure over said semiconductor substrate;  
a passivation layer over said metallization structure, wherein an opening in said  
passivation layer exposes a top surface of said metallization structure; and  
10 a patterned circuit layer comprising a first portion connected to said top surface  
through said opening, ~~wherein said patterned circuit layer comprises a first portion and~~  
used to have a bump formed thereover, a second portion ~~comprising a gold layer used to~~  
be in contact with a testing probe, and a third portion used to be wirebonded thereto,  
wherein ~~said gold layer is used to be in contact with a testing probe, and wherein said first~~  
15 portion is connected to said second portion.

Claim 2 (canceled)

- 20 3. (currently amended) The chip circuit component of Claim 1, wherein said second  
portion comprises a gold layer having ~~has~~ a thickness of greater than 1 micron.

Claim 4 (canceled)

- 25 5. (currently amended) The chip circuit component of Claim 1, wherein said patterned  
circuit layer comprises a gold layer and a nickel layer under said gold layer.

6. (currently amended) The chip circuit component of Claim 1, wherein said patterned

circuit layer comprises a gold layer and a copper layer under said gold layer.

7. (currently amended) The ~~chip circuit component~~ of Claim 1, wherein said patterned circuit layer further comprises a copper layer, ~~and a nickel layer over said copper layer,~~  
5 and ~~wherein said a gold layer is over said nickel layer.~~

8. (previously presented) The ~~chip circuit component~~ of Claim 1 further comprising a polymer layer between said passivation layer and said patterned circuit layer.

10 9. (previously presented) The ~~chip circuit component~~ of Claim 8, wherein said polymer layer comprises polyimide.

10. (previously presented) The ~~chip circuit component~~ of Claim 1 further comprising a polymer layer on said patterned circuit layer, multiple openings in said polymer layer  
15 exposing said first and second portions.

11. (previously presented) The ~~chip circuit component~~ of Claim 10, wherein said polymer layer comprises polyimide.

20 Claim 12 (canceled)

13. (currently amended) The ~~chip circuit component~~ of Claim 1, wherein said patterned circuit layer comprising a metal trace line connecting said first and second portions.

25 Claim 14 (canceled)

15. (previously presented) The ~~chip circuit component~~ of Claim 1, wherein said passivation layer comprises a topmost nitride layer of said circuit component.

16. (previously presented) The ~~chip circuit component~~ of Claim 1, wherein said passivation layer has a thickness of greater than 0.35  $\mu\text{m}$ .
- 5 17. (currently amended) The ~~chip circuit component~~ of Claim 1 further comprising a bump over ~~on~~ said first portion.
18. (previously presented) The ~~chip circuit component~~ of Claim 17 further comprising a nickel layer between said bump and said first portion.
- 10 19. (previously presented) The ~~chip circuit component~~ of Claim 17, wherein said bump comprises solder.
20. (previously presented) The ~~chip circuit component~~ of Claim 17 further comprising a copper layer between said bump and said first portion.
- 15 21. (previously presented) The ~~chip circuit component~~ of Claim 17, wherein said bump comprises a lead-free alloy.
- 20 Claims 22 and 23 (canceled)
24. (previously presented) The ~~chip circuit component~~ of Claim 1, wherein said patterned circuit layer comprises a metal trace connecting said second and third portions.
- 25 25. (previously presented) The ~~chip circuit component~~ of Claim 1, wherein a pitch between said first and second portions is less than 300  $\mu\text{m}$ .
26. (previously presented) The ~~chip circuit component~~ of Claim 1, wherein a pitch

between said first and second portions is less than 1 millimeter.

27. (currently amended) A chip circuit component comprising:

- a semiconductor substrate;
- 5 a metallization structure over said semiconductor substrate;
- a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a top surface of said metallization structure; and
- a patterned circuit layer comprising a metal trace over said passivation layer and  
connected to said top surface through said opening, ~~wherein said patterned circuit layer~~  
10 ~~comprises~~ a first portion used to have a bump formed thereover and connected to said  
metal trace, and a second portion comprising a copper layer, ~~wherein said copper layer is~~  
used to be wirebonded thereover.

28. (currently amended) The chip circuit component of Claim 27, wherein said second  
15 portion patterned circuit layer further comprises a titanium-containing layer under said copper layer.

29. (currently amended) The chip circuit component of Claim 27, wherein said second  
portion patterned circuit layer further comprises a chromium-containing layer under said  
20 copper layer.

30. (currently amended) The chip circuit component of Claim 27 further comprising a polymer layer between said passivation layer and said patterned circuit layer.

- 25 31. (currently amended) The chip circuit component of Claim 30, wherein said polymer layer comprises polyimide.

32. (currently amended) The chip circuit component of Claim 27 comprising a polymer

layer on said patterned circuit layer, multiple openings in said polymer layer exposing said first and second portions.

33. (currently amended) The chip circuit component of Claim 32, wherein said polymer  
5 layer comprises polyimide.

34. (currently amended) The chip circuit component of Claim 27, wherein said ~~patterned circuit layer comprises a metal~~ trace connects ~~line connecting~~ said first and second  
10 portions.

35. (currently amended) The chip circuit component of Claim 27, wherein said patterned circuit layer comprises a third portion used to be in contact with a testing probe.

Claim 36 (canceled)  
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37. (currently amended) The chip circuit component of Claim 35, wherein said ~~patterned circuit layer comprises a metal trace~~ connects ~~connecting~~ said first and third portions.

38. (currently amended) The chip circuit component of Claim 27, wherein said  
20 passivation layer has a thickness of greater than 0.35  $\mu\text{m}$ .

39. (currently amended) The chip circuit component of Claim 27, wherein said passivation layer comprises a topmost nitride layer of said circuit component.

40. (currently amended) The chip circuit component of Claim 27 further comprising a  
25 bump over said first portion.

41. (currently amended) The chip circuit component of Claim 40, wherein said bump

comprises solder.

42. (currently amended) The ~~chip circuit component~~ of Claim 40 further comprising a nickel layer between said bump and said first portion.

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43. (currently amended) The ~~chip circuit component~~ of Claim 40, wherein said bump comprises a lead-free alloy.

44. (currently amended) The ~~chip circuit component~~ of Claim 27 further comprising a wirebonded wire bonded over said second portion.

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Claims 45-50 (canceled)

51. (currently amended) The ~~chip circuit component~~ of Claim 27, wherein said second portion further comprises a nickel layer over said copper layer, ~~and wherein said nickel layer is used to be said wirebonded thereover.~~

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52. (currently amended) The ~~chip circuit component~~ of Claim 27, wherein said second portion further comprises a gold layer over said copper layer, ~~and wherein said gold layer is used to be said wirebonded thereon.~~

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53. (new) The chip of Claim 27, wherein said metal trace comprises a copper layer.

54. (new) The chip of Claim 53, wherein said metal trace further comprises a nickel layer over said copper layer of said metal trace.

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55. (new) The chip of Claim 54, wherein said metal trace further comprises a gold layer over said nickel layer.

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56. (new) The chip of Claim 27, wherein said first portion comprises a copper layer.
57. (new) The chip of Claim 56, wherein said first portion further comprises a nickel layer  
5 over said copper layer of said first portion.
58. (new) The chip of Claim 57, wherein said metal trace further comprises a gold layer  
over said nickel layer.
- 10 59. (new) The chip of Claim 1, wherein said second portion comprises a gold layer.